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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Lindstedt	Docket No.:	2002 P 16328 US
Serial No:	10/788,805	Art Unit:	2811
Date Filed:	February 27, 2004	Examiner:	Hung Vo
Title:	Semiconductor Chip Arrangement and a Method for Its Production		

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- Certification of Facsimile Transmission (1 page)
- Replacement Appeal Brief (27 pages)

Respectfully submitted,

Nancy Milinkovich

Nancy Milinkovich
Legal Assistant

Confirmation Respectfully Requested

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Alexandria, VA 22313-1450

REPLACEMENT APPEAL BRIEF

Dear Sir:

This replacement brief is filed in response to the Notice of Non-Compliant Appeal Brief, mailed on November 21, 2006. The original brief was filed on November 2, 2006 in response to the Final Rejection mailed on February 24, 2006. That brief was indicated as being defective for failing to provide the status of all claims. This brief corrects this oversight.

REAL PARTY OF INTEREST (37 C.F.R. 41.37(c)(1)(i))

The present application is assigned to Infineon Technologies AG.

RELATED APPEALS AND INTERFERENCES (37 C.F.R. 41.37(c)(1)(ii))

Appellant is not aware of any related appeals or interferences.

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STATUS OF CLAIMS (37 C.F.R. 41.37(c)(1)(iii))

Claims 1-7, 9-13 and 20-27 stand finally rejected. No claims have been allowed. Therefore, claims 1-7, 9-13 and 20-27 are the subject of this appeal. Claims 8 and 14-19 have been canceled. The claims on appeal are reproduced in the Claims Appendix.

STATUS OF AMENDMENTS (37 C.F.R. 41.37(c)(1)(iv))

An Amendment under 37 CFR §1.116 was filed on April 24, 2006. This amendment was filed in an attempt to avoid the time and cost of this appeal. The amendment attempted to add the limitations of dependent claims 5 and 24 to independent claims 1 and 20 but was not entered because it allegedly raised new issues with regard to the remaining claims that separately depend from claims 1 and 20. Since the original goal of avoiding this appeal has been unsuccessful, all claims are on appeal here.

A Pre-Appeal Brief Request for Review was filed on June 26, 2006.

SUMMARY OF CLAIMED SUBJECT MATTER (37 C.F.R. 41.37(c)(1)(v))

The present invention relates to an arrangement of multiple unpackaged semiconductor substrates. The subject matter of each of the three embodiments claimed in the independent claims will now be discussed with reference to the specification and drawings.

Figure 2C, which is reproduced below, provides an example of the embodiment of claim 1. Referring to this figure, a semiconductor chip arrangement includes a mount element 1. Par. 42, line 2. A first semiconductor substrate 2 includes at least one interconnect 10 (shown in Fig. 2B) formed on the first semiconductor substrate 2 and also includes at least one contact area 8 that is electrically connected to the interconnect 10 and is arranged on a side surface 12 (labeled in Fig. 2B) of the first semiconductor substrate. Similarly, a second semiconductor substrate 3 has at least

one interconnect 10 formed on the second semiconductor substrate and also includes at least one contact area 8 that is electrically connected to the interconnect 10 and is arranged on a side surface of the second semiconductor substrate 3. Par. 42, line 4.

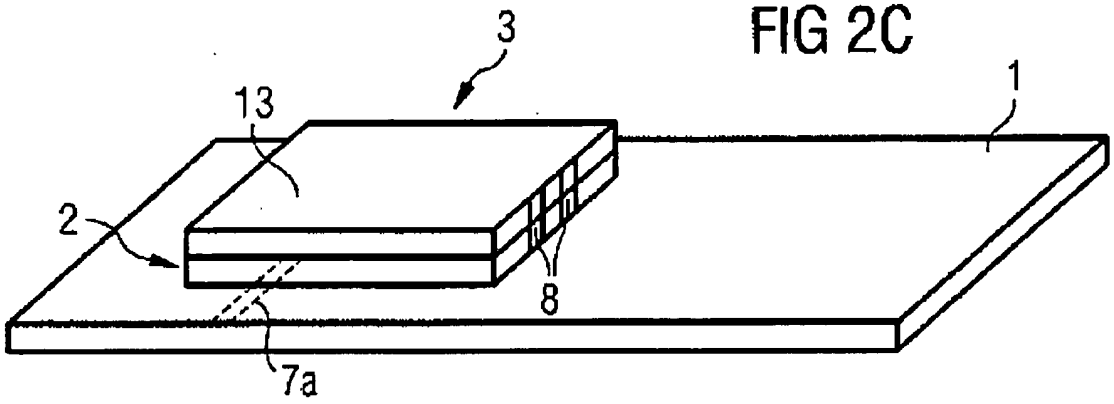


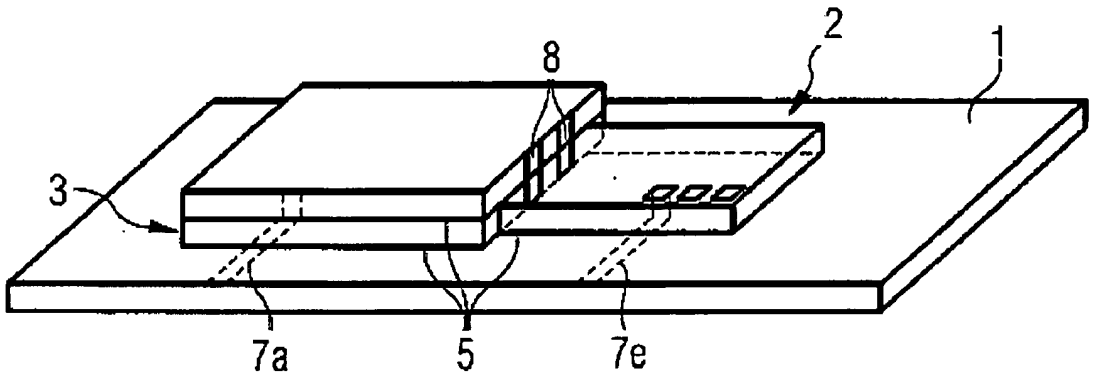
FIG 2C

The second semiconductor substrate 3 is arranged on the first semiconductor substrate 2 while the first semiconductor substrate 2 is arranged on the mount element 1. Par. 43, lines 1, 4. In the claimed configuration, a first main surface of the second semiconductor substrate 3 rests on the first semiconductor substrate 2, and a first main surface of the first semiconductor substrate 2 rests on the mount element 1. Par. 43, lines 1, 4. An electrical contact is produced between the contact area 8 on the first semiconductor substrate 2 and the contact area 8 on the second semiconductor substrate 3. Par. 43, line 6. Both the first and second semiconductor substrates are unpackaged semiconductor chips with integrated circuitry disposed therein. Par. 41, line 1; Par. 35, line 2.

In several embodiments, e.g., those claimed in claims 5, 11 and 24, the side contact areas 8 on the first semiconductor substrate 2 and on the second semiconductor substrate 3 each extend from the first main surface to a second main surface of the respective semiconductor substrate. Par. 43, line 7. This feature is illustrated in Figure 2C above.

The embodiment of claim 7 is similar to the embodiment of claim 1 but includes a further semiconductor substrate arranged on the mount element alongside the lower of the stacked semiconductor substrates. An exemplary embodiment of this configuration is shown in Figure 3B, which is reproduced below.

FIG 3B



In terms of the claim language, the embodiment includes a semiconductor chip arrangement including a mount element 1. Par 45, line 2. A first semiconductor substrate 2 is arranged over a surface of the mount element 1. Par. 45, line 2. As before, the first semiconductor substrate 2 includes at least one interconnect 10 (not shown in Fig. 3B, see Fig. 3A) formed thereon. Par. 44, line 2. The first semiconductor substrate 2 further includes at least one contact area 8 that is electrically connected to the interconnect 10 and is arranged along a side surface 12 (not labeled in Fig. 3B, see Fig. 3A) of the first semiconductor substrate 2. Par. 45, line 6.

A second semiconductor substrate 3 arranged over the surface of the mount element 1 alongside the first semiconductor substrate 2. Par. 45, line 2. As with the first substrate 2, the second semiconductor substrate 3 includes at least one interconnect 10 and at least one contact area 8. Par. 44, line 2; par. 45, line 6. The second semiconductor substrate 3 is arranged so that an

electrical contact is produced between the contact area 8 of the first semiconductor substrate 2 and the contact area 8 of the second semiconductor substrate 3. Par. 45, line 3.

This embodiment also includes a third semiconductor substrate 9 (labeled in Fig. 3A) arranged over the second semiconductor substrate 3. Par. 46, line 1. As with the first and second substrates, the third semiconductor substrate includes at least one interconnect 10 and at least one contact area 8 arranged along a side surface 12. Par. 46, line 3. The third semiconductor substrate is arranged so that an electrical contact is produced between the contact area 8 of the third semiconductor substrate 9 and the contact area 8 of the second semiconductor substrate 3. Par. 46, line 3.

The first, second and third semiconductor substrates 2, 3 and 9 each comprise unpackaged semiconductor chips with integrated circuitry disposed in the area of a first main surface such that the integrated circuit is electrically coupled to the interconnect. Par. 41, line 1; par. 35, line 2. The first main surface is parallel to the surface of the mount element. Fig. 3B.

The embodiment of claim 20, the final independent claim, is also illustrated in Figure 3B. *See also* Fig. 1C. In this embodiment, a semiconductor chip arrangement includes a mount element 1. Par. 33, line 2. A first semiconductor substrate 2 is arranged over a surface of the mount element 1. Par. 33, line 2. Once again, the first semiconductor substrate 2 includes at least one interconnect 10 formed thereon. Par. 35, line 4. The first semiconductor substrate 2 further includes at least one contact area 8 that is electrically connected to the interconnect 10 and is arranged along a side surface 12 of the first semiconductor substrate 2. Par. 35, line 3.

A second semiconductor substrate 3 is arranged over the surface of the mount element 1 alongside the first semiconductor substrate 2. Par. 37, line 2. Yet again, the second semiconductor substrate 3 includes at least one interconnect 10 and at least one contact area 8 that is electrically

connected to the interconnect 10 and is arranged along a side surface of the second semiconductor substrate. Par. 35, line 4; par. 35, line 3. The second semiconductor substrate 3 is arranged so that an electrical contact is produced between the contact area 8 of the first semiconductor substrate 2 and the contact area 8 of the second semiconductor substrate 3. Par. 37, line 4.

As with all of the claimed embodiments, the first, and second semiconductor substrates 2 and 3 each comprise an unpackaged semiconductor substrate having integrated circuitry disposed in the area of a first main surface. Par. 41, line 1; par. 35, line 2. The first main surface is parallel to the surface of the mount element 1.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL (37 C.F.R. 41.37(c)(1)(vi))

(1) Claims 1-4 and 26 stand rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,834,162 (hereinafter "Malba").

(2) Claims 5-7, 9-13, 20-25 and 27 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Malba in view of U.S. Patent No. 6,518,659 (hereinafter "Glenn").

ARGUMENT (37 C.F.R. 41.37(c)(1)(vii))

It is respectfully submitted that claims 1-7, 9-13 and 20-27 recite patentable subject matter under the provisions of 35 U.S.C. §§ 102 and 103. Each of the claims will be discussed in turn. Any claim not explicitly argued stands or falls with the claim from which it depends.

1. Claim 1 is not anticipated by Malba

Claim 1 specifically recites that "the second semiconductor substrate is arranged on the first semiconductor substrate ... wherein an electrical contact is produced between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate."

Appellant respectfully submits that the Malba patent does not teach or suggest the limitations of claim 1.

Malba teaches an unpackaged semiconductor chip with a contact area 17 arranged on a sidewall 12 of a substrate 10. While Malba teaches a stack of semiconductor chips, the reference does not teach an electrical connection between contact areas 17 of various ones of the chips.

The Final Rejection provides no citation to a portion of Malba that teaches the above-quoted portion of the claim. Further, Appellant has studied the reference and finds no teaching of an electrical contact between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate.

Looking at the detailed description of the patent, Malba states that "[w]ith the I/O pads routed onto the sidewall, they are readily available for attachment to a desired location." Col. 2, lines 62-64. The patent provides no indication as to where this desired location might be. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." MPEP § 2131, quoting *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). In this case, the limitation in question is neither expressly nor inherently taught.

Similarly, Malba teaches

> FIG. 3 illustrates an exploded stack of chips 10 having L-connects 14 extending from bond pads 13 to only one sidewall 12, with bond pads 17 formed thereon. It is readily seen that when the chips 10 of FIG. 3 are stacked one on top of another electrical interconnects between the sidewall bond pads 17, or the interconnect portions on the sidewalls if bond pads are omitted, of the various chips can be easily made. Also, with the chips stacked, packaging of the stacked chips with other chips or desired component can be readily accomplished due to the sidewall bond pads 17.

Col. 4, lines 18-27.

In this paragraph, Malba states that electrical interconnects between the sidewall bond pads 17 of the various chips can be made. Claim 1, on the other hand, requires an electrical contact between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate. Malba does not anticipate claim 1 because the reference does not state where the electrical interconnects are between. While they could be between a first chip and a second chip, they could also be between the chips and a third component. Once again, the claim limitation is not expressly or inherently taught and, therefore, the claim cannot be anticipated.

2. Claim 3 is not anticipated by Malba

Claim 3 depends from claim 1 and further requires "a conductive material applied between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate." As stated above with respect to claim 1, Malba does not teach any electrical contact between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate. Malba certainly does not teach that such an electrical contact could be made with a conductive material applied between the contact areas as required by claim 3.

In discussing claim 3, the final rejection states that Malba discloses a conductive material 13 applied between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate. Review of the reference, however, makes clear that conductive material 13 is a bond pad on the upper surface of the chip. Col. 4, line 5. While the bond pad 13 on the upper surface of each chip is coupled to the bond pad 17 on the side surface of that chip (*see* col. 4, lines 18-20), the reference does not teach that the bond pad 13 is applied between the contact area (bond pad 17) on that chip and the contact area of another chip.

As a result, claim 3 is independently allowable over the references of record.

3. Claim 4 is not anticipated by Malba

Claim 4 depends from claim 1 and further limits that claim by requiring that "the first main surface of the first semiconductor substrate is attached to the mount element." Malba does not teach or suggest this limitation.

Claim 1 requires a "mount element." In rejecting this claim, the Final Rejection points to the "substrate" discussed at column 4, lines 28-41 or the bottom chip 10 in Figure 3. Initially, Appellant points out that the substrate discussed in the operational sequence cannot be a mount element as required by claim 1. This substrate is a temporary holding device and is never configured with the first and second semiconductor substrates as required by the claim. While the chips are adhered to the substrate in column 4, line 33, they are later removed as discussed at column 5, line 36.

The entire discussion referred to in the Final Rejection relates to "a specific operational sequence for forming the L-connects [14] and sidewall bond pads [17] on integrated circuit chips." Col. 4, line 28. This operational sequence is complete long before the chips are stacked. As a result, the fact that one of the chips was at one time adhered in a temporary handling arrangement has no bearing as to whether the reference teaches the first main surface of the first semiconductor substrate being attached to a mount element.

As an alternative, the Final Rejection refers to Figure 3 to state the lowest chip 10 can serve as a mount element. Appellant agrees that the term "mount element" is broad enough to include this chip. The reference, however, provides no indication that the first main surface of the middle chip 10 is attached to the lowest chip 10. Certainly, the chips are stacked. Col. 4, line 25. The fact

that the chips are stacked, however, does not necessarily lead to the first main surface of one chip being attached to another chip.

As examples, the present specification teaches that the first semiconductor substrate may be fixed on the mount element by means of an adhesive or via electrical contacts, for example by means of soldered joints, or may be attached to the mount element by means of mechanical joints. Par. 23. Malba teaches no such examples.

As a result, claim 3 is independently allowable over the references of record.

4. Claim 5 is not obvious over Malba in view of Glenn

Claim 5 depends upon claim 1 and further requires that "the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate each extend from the first main surface to a second main surface of the respective semiconductor substrate." The references of record do not teach or suggest the limitations of claim 5.

As discussed above, Malba teaches an unpackaged semiconductor chip with a contact area 17 arranged on a sidewall 12 of a substrate 10. Undisputedly, Malba does not teach that the contact area 17 extends from the first main surface to the second main surface.

Glenn teaches packages 10 that include metal leads 21 alongside the outside of the package and are formed from the leadframe used in the packaging process. These leads 21 extend from a first main surface of the package to a second main surface of the package. *See* Fig. 1. The packages are electrically interconnected.

The contents of the two cited references do not provide any suggestion for combining their technical teaching since Glenn refers to a packaged semiconductor substrate surrounded by a housing and Malba refers to an unpackaged semiconductor substrate. It is not apparent how one of

ordinary skill in the art would apply the electrical contacts 21 of Glenn to the unpackaged chip of Malba. In Glenn, the contacts are formed during the packaging process. These contacts surround a sidewall of the housing, which is much larger and higher than an unpackaged semiconductor substrate. It would not be obvious to modify an unpackaged semiconductor substrate or chip having much smaller dimensions, in particular in vertical direction perpendicular to the semiconductor main surfaces, with these teachings.

The Examiner and Appellant both agree that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. In other words, the legal principle is not at issue here, only its application to the facts of this case.

In the advisory action, the Examiner argues that one of ordinary skill in the art would be motivated to form the structure of Malba as modified by Glenn "in order to easily add more semiconductor substrate/chip to increase the circuit density without increasing the mounting area on a printed circuit board." Unfortunately, the combination of references provides no teaching as to how this goal could be achieved. The present invention is the only teaching of interconnected, stacked, unpackaged semiconductor substrates and, it goes without saying, Appellant 's own teachings cannot provide the motivation for combining the references.

Appellant respectfully submits that one of ordinary skill in the art would not be able to use the leads of Glenn with the unpackaged semiconductor chips of Malba. As taught by Glenn, the leads 21 are portions of a lead frame 61. Col. 11, line 38. *See also*, Fig. 7, which shows an array of four leadframes. The leadframe 61 is encapsulated with molding compound that does not cover portions 24 of the leads 21. Col. 11, line 23. After encapsulation, the dambar portion of the

leadframe is removed from the package, which includes lead 21. Col. 11, line 50. The leads 21 may be dipped in solder or plated with solder for electrical interconnection to a printed circuit board or to abutting leads of other packages. Col. 11, line 54.

Appellant respectfully submits that once this packaging process is applied to an unpackaged chip, the chip is no longer unpackaged. Glenn provides no teaching or suggestion that leads 21 could be formed by any method other than by packaging the integrated circuit 28. Once the integrated circuit is packaged, it is no longer within the scope of the claim. As a result, the references cannot be combined.

Even if one could form the leads 21 on an unpackaged chip, doing so would be detrimental to the Malba configuration. Malba teaches contacts 17 along sidewalls 12 of an integrated circuit. "With the I/O pads routed onto the sidewall, they are readily available for attachment to a desired location." Col. 2, line 63. Leads along the sidewalls, however, would cover these I/O pads so that they are no longer readily available for attachment. In other words, the configuration of leads taught by Glenn is incompatible with Malba's chip configuration. This fact provides another reason why combination of the two references is not obvious.

Taking it a step further, if Malba did desire to interconnect ones of the chips in the stack and could include the sidewall leads taught by Glenn, then the side contacts 17 would be rendered useless. Since Glenn already teaches an unpackaged chip and a goal of coupling that chip to another chip in the stack, Malba would not add any information to the analysis. The issue then is whether it would be obvious to modify Glenn to include only the chips 28 and the leads 21 without the package body 11.

Glenn explicitly states the Examiner's motivating goal of increasing the circuit density without increasing the mounting area on a printed circuit board. "Stacking the packages allows an

increase in the density of packages on a printed circuit board without a corresponding increase in the area of the printed circuit board consumed thereby." Col. 1, line 39. If it was obvious to apply Glenn's leads 21 to the unpackaged chip 28, Glenn would have done so. This configuration improves the stated goal of increasing density. As a result, one can only conclude that this modification is not obvious.

As a result, claim 5 is independently allowable over the references of record.

5. Claim 7 is not obvious over Malba in view of Glenn

Independent claim 7 recites a third semiconductor substrate arranged over a second semiconductor substrate. The third semiconductor substrate includes at least one contact area arranged along a side surface so that an electrical contact is produced between the contact area of the third semiconductor substrate and the contact area of the second semiconductor substrate. The portion of the claim is substantively identical to what was discussed earlier with respect to claim 1. As a result, allowance of claim 1 will necessarily lead to allowance of claim 7.

In addition to the stacked substrates (enumerated as the second and third substrates), claim 7 also requires two substrates (enumerated as the first and second substrates) alongside each other on the mount element. In particular, the claim recites "a second semiconductor substrate arranged over the surface of the mount element alongside the first semiconductor substrate, ... the second semiconductor substrate further including at least one contact area ... arranged along a side surface of the second semiconductor substrate, the second semiconductor substrate arranged so that an electrical contact is produced between the contact area of the first semiconductor substrate and the contact area of the second semiconductor substrate." The combination of Malba and Glenn does not teach or suggest this limitation.

As admitted in the Final Rejection, Malba does not show the second semiconductor arranged so that an electrical contact is produced between the contact areas as claimed. Appellant admits that Glenn teaches two packaged chips alongside one another with side contacts that are electrically connected. *See e.g.*, Figure 6c or 6d. The two references, however, do not teach the limitations because 1) the references are not properly combinable and 2) neither reference teaches the mount element required by claim 7.

The first issue, whether the references are combinable, was discussed in great detail above with respect to claim 5. As a result, this discussion will not be repeated here. As stated above, it would not be obvious to process an unpackaged substrate in a manner taught for packaged chips. Further, doing so would eliminate the need for the sidewall pads 17 taught by Malba. If Malba could be used with the C-leads 21 taught by Glenn, the sidewall pads 17 would be rendered useless. Conversely, if Glenn could have used the C-leads on unpackaged chips, he would have done so because it further enhances his stated goal of maximizing density.

Claim 7 includes a mount element that is not taught by the references individually or in combination. Specifically, claim 7 states that "a first semiconductor substrate [is] arranged over a surface of the mount element" and "a second semiconductor substrate [is] arranged over the surface of the mount element alongside the first semiconductor substrate." Neither reference teaches or suggests a mount element with two substrates arranged alongside one another. In fact, the Final Rejection simply fails to mention this element.

Going back to the references themselves, Malba teaches a temporary holding arrangement used during the processing of the chips. As discussed above with respect to claim 4, this temporary holding device is never configured with the first, second and third semiconductor substrates as

required by the claim. The individual chips are processed and then removed from the substrate. Col. 4, line 33 – col. 5, line 36.

Further, as also discussed above, the present application includes no limitation preventing a semiconductor substrate or packaged chip from serving as the mount element. Neither of the references, however, teach or suggest two semiconductor substrates arranged over the surface of an additional semiconductor substrate (or packaged chip). For example, Figure 6d of Glenn, clearly shows two stacks of packages. Col. 5., line 48. None of the bottommost packages, however, includes both a first semiconductor substrate and a second semiconductor substrate arranged over a surface thereof.

For all these reasons, it is respectfully submitted that claim 7 is allowable over the references of record.

6. Claim 9 is not obvious over Malba in view of Glenn

Claim 9 depends from claim 7 and further recites "a conductive material applied between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate." Neither Malba nor Glenn teach or suggest this limitation.

The Final Rejection states that Malba and Glenn disclose a conductive material 14. Since numeral 14 in Glenn refers to a side surface of a package 10, Appellant assumes that the rejection refers to the L-connect 14 of Malba. This L-connect 14, however, couples the top surface bond pad of a chip to the sidewall bond pad 17 of that same chip. This material is in no way a conductive material applied between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate.

As a result, claim 9 is independently allowable over the references of record.

7. Claim 11 is not obvious over Malba in view of Glenn

Claim 11 depends from claim 7 and further requires that "the contact areas on the first and the second semiconductor substrates each extend from a first main surface to a second main surface of the respective semiconductor substrate." Appellant respectfully submits that the references of record do not teach or suggest the limitations of claim 11.

As discussed above with respect to claim 5, it would not be obvious to process an unpackaged substrate in a manner taught for packaged chips. Further, doing so would eliminate the need for the sidewall pads 17 taught by Malba. If Malba could be used with the C-leads 21 taught by Glenn, the sidewall pads 17 would be rendered useless. Conversely, if Glenn could have used the C-leads on unpackaged chips, he would have done so because it further enhances his stated goal of maximizing density.

As a result, claim 11 is independently allowable over the references of record.

8. Claim 20 is not obvious over Malba in view of Glenn

Independent claim 20 specifically recites "a first semiconductor substrate arranged over a surface of the mount element" and "a second semiconductor substrate arranged over the surface of the mount element alongside the first semiconductor substrate." The combination of Malba and Glenn does not teach or suggest a mount element underlying first and second substrates.

As discussed above with respect to claim 7, the two references do not teach the limitations because 1) the references are not properly combinable and 2) neither reference teaches the mount element required by claim 20. To simplify this brief, the arguments will not be repeated. Rather reference can be made to the discussion above.

It is therefore respectfully submitted that claim 20 is allowable over the references of record.

9. Claim 22 is not obvious over Malba in view of Glenn

Claim 22 depends from claim 20 and further includes "a conductive material applied between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate." As discussed above with respect to claim 9, the references of record do not teach or suggest the limitations of claim 22.

The Final Rejection states that Malba and Glenn disclose a conductive material 14. Since numeral 14 in Glenn refers to a side surface of a package 10, Appellant assumes that the rejection refers to the L-connect 14 of Malba. This L-connect 14, however, couples the top surface bond pad of a chip to the sidewall bond pad 17 of that same chip. This material is in no way a conductive material applied between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate.

As a result, claim 11 is independently allowable over the references of record.

10. Claim 24 is not obvious over Malba in view of Glenn

Claim 24 depends from claim 20 and further requires that "the contact areas on the first and the second semiconductor substrates each extend from a first main surface to a second main surface of the respective semiconductor substrates." Appellant respectfully submits that the references of record do not teach or suggest the limitations of claim 24.

As discussed above with respect to claim 5, it would not be obvious to process an unpackaged substrate in a manner taught for packaged chips. Further, doing so would eliminate the need for the sidewall pads 17 taught by Malba. If Malba could be used with the C-leads 21 taught by Glenn, the sidewall pads 17 would be rendered useless. Conversely, if Glenn could have used

the C-leads on unpackaged chips, he would have done so because it further enhances his stated goal of maximizing density.

As a result, claim 24 is independently allowable over the references of record.

11. Claim 27 is not obvious over Malba in view of Glenn

Claim 27 depends from claim 7 and further requires that "the first semiconductor substrate [is] arranged in direct contact with the surface of the mount element [and] the second semiconductor substrate [is] arranged in direct contact with the surface of the mount element." The limitations of claim 27 are not taught or suggested by the references of record.

The Final Rejection provides no citation to any portion of the references that teach or suggest the limitations of claim 27. The rejection does, however, admit that Malba does not show first and second substrates over a mount element. As discussed above, Glenn teaches packages arranged alongside one another. Even if these packages are over a mount element, the semiconductor substrates are not in direct contact with a surface of the mount element.

Referring to Figure 6d of Glenn, each package (labeled 10 in Figure 6c) includes a semiconductor substrate 28, which is defined in the claim as an unpackaged semiconductor chip with integrated circuitry disposed in the area of a first main surface. These chips are clearly enclosed within a package. As a result, the integrated circuit 28 of the middle package is never in direct contact with the package 10 beneath it. Rather the packaging portion of the middle chip is in direct contact with the lower package.

As a result, claim 27 is independently allowable over the references of record.

CONCLUSION

For the foregoing reasons, Appellant respectfully submits that the final rejection of claims 1-4 and 25 under 35 U.S.C. § 102 and claims 5-7, 9-13, 20-25 and 27 under 35 U.S.C. § 103 is improper and respectfully requests that the Board of Patent Appeals and Interference so find and reverse these rejections.

Applicant has made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Ira S. Matsil, Applicant's attorney, at 972-732-1001 so that such issues may be resolved as expeditiously as possible. No fee is believed due in connection with this filing. However, should one be deemed due, the Commissioner is hereby authorized to charge Deposit Account No. 50-1065.

Respectfully submitted,

Ira S. Matsil
Attorney for Appellant
Reg. No. 35,272

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CLAIMS APPENDIX

1. A semiconductor chip arrangement comprising:

a mount element;

a first semiconductor substrate including at least one interconnect formed on the first semiconductor substrate and also including at least one contact area that is electrically connected to the interconnect and is arranged on a side surface of the first semiconductor substrate; and

a second semiconductor substrate having at least one interconnect formed on the second semiconductor substrate and also including at least one contact area that is electrically connected to the interconnect and is arranged on a side surface of the second semiconductor substrate;

wherein the second semiconductor substrate is arranged on the first semiconductor substrate and the first semiconductor substrate is arranged on the mount element such that a first main surface of the second semiconductor substrate rests on the first semiconductor substrate, and a first main surface of the first semiconductor substrate rests on the mount element, and wherein an electrical contact is produced between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate and wherein the first and second semiconductor substrates each comprise an unpackaged semiconductor chip with integrated circuitry disposed therein.

2. The semiconductor chip arrangement of claim 1 wherein the first and second semiconductor substrates each have the integrated circuitry disposed in the area of the first main surface, wherein, for both the first and second semiconductor substrates, the integrated circuitry is electrically coupled to the interconnect.

3. The semiconductor chip arrangement of claim 1 and further comprising a conductive material applied between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate.

4. The semiconductor chip arrangement of claim 1 wherein the first main surface of the first semiconductor substrate is attached to the mount element.

5. The semiconductor chip arrangement of claim 1 wherein the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate each extend from the first main surface to a second main surface of the respective semiconductor substrate.

6. The semiconductor chip arrangement of claim 1 wherein each of the first and second semiconductor substrates includes a dynamic random access memory formed therein.

7. A semiconductor chip arrangement comprising:

a mount element;

a first semiconductor substrate arranged over a surface of the mount element, the first semiconductor substrate including at least one interconnect formed thereon, the first semiconductor substrate further including at least one contact area that is electrically connected to the interconnect and is arranged along a side surface of the first semiconductor substrate;

a second semiconductor substrate arranged over the surface of the mount element alongside the first semiconductor substrate, the second semiconductor substrate including at least one interconnect formed thereon, the second semiconductor substrate further including at least one contact area that is electrically connected to the interconnect and is arranged along a side surface of the second semiconductor substrate, the second semiconductor substrate arranged so that an

electrical contact is produced between the contact area of the first semiconductor substrate and the contact area of the second semiconductor substrate; and

a third semiconductor substrate arranged over the second semiconductor substrate, the third semiconductor substrate including at least one interconnect formed thereon, the third semiconductor substrate further including at least one contact area that is electrically connected to the interconnect and is arranged along a side surface of the third semiconductor substrate, the third semiconductor substrate arranged so that an electrical contact is produced between the contact area of the third semiconductor substrate and the contact area of the second semiconductor substrate;

wherein the first, second and third semiconductor substrates each comprise unpackaged semiconductor chips with integrated circuitry disposed in the area of a first main surface such that the integrated circuit is electrically coupled to the interconnect, the first main surface being parallel to the surface of the mount element.

8. (Canceled)

9. The semiconductor chip arrangement of claim 7 and further comprising a conductive material applied between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate.

10. The semiconductor chip arrangement of claim 7 wherein the first semiconductor substrate is attached to the mount element and wherein the second semiconductor substrate is attached to the mount element.

11. The semiconductor chip arrangement of claim 7 wherein the contact areas on the first and the second semiconductor substrates each extend from a first main surface to a second main surface of the respective semiconductor substrate.

12. The semiconductor chip arrangement of claim 11 wherein the contact area on the third semiconductor substrate extends to a first main surface on the third semiconductor substrate.

13. The semiconductor chip arrangement of claim 7 wherein the integrated circuitry of each of the first, second, and third semiconductor substrates includes a dynamic random access memory.

14–19. (Canceled)

20. A semiconductor chip arrangement comprising:

a mount element;

a first semiconductor substrate arranged over a surface of the mount element, the first semiconductor substrate including at least one interconnect formed thereon, the first semiconductor substrate further including at least one contact area that is electrically connected to the interconnect and is arranged along a side surface of the first semiconductor substrate; and

a second semiconductor substrate arranged over the surface of the mount element alongside the first semiconductor substrate, the second semiconductor substrate including at least one interconnect formed thereon, the second semiconductor substrate further including at least one contact area that is electrically connected to the interconnect and is arranged along a side surface of the second semiconductor substrate;

wherein the second semiconductor substrate is arranged so that an electrical contact is produced between the contact area of the first semiconductor substrate and the contact area of the

second semiconductor substrate; and

wherein the first, and second semiconductor substrates each comprise an unpackaged semiconductor substrate having integrated circuitry disposed in the area of a first main surface, the first main surface being parallel to the surface of the mount element.

21. The semiconductor chip arrangement of claim 20, wherein each of the semiconductor substrates the integrated circuitry is electrically coupled to the interconnect.

22. The semiconductor chip arrangement of claim 20 and further comprising a conductive material applied between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate.

23. The semiconductor chip arrangement of claim 20 wherein the first semiconductor substrate is attached to the mount element and wherein the second semiconductor substrate is attached to the mount element.

24. The semiconductor chip arrangement of claim 20 wherein the contact areas on the first and the second semiconductor substrates each extend from a first main surface to a second main surface of the respective semiconductor substrates.

25. The semiconductor chip arrangement of claim 20 wherein each of the first and second semiconductor substrates includes a dynamic random access memory formed therein.

26. The semiconductor chip arrangement of claim 1, wherein the second semiconductor substrate is arranged in direct contact with the first semiconductor substrate and the first semiconductor substrate is arranged in direct contact with the mount element.

27. The semiconductor chip arrangement of claim 7, wherein the first semiconductor substrate arranged in direct contact with the surface of the mount element, the second semiconductor substrate arranged in direct contact with the surface of the mount element, and the third semiconductor substrate arranged in direct contact with the second semiconductor substrate.

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None